

Memory Safety for Telecommunication Systems



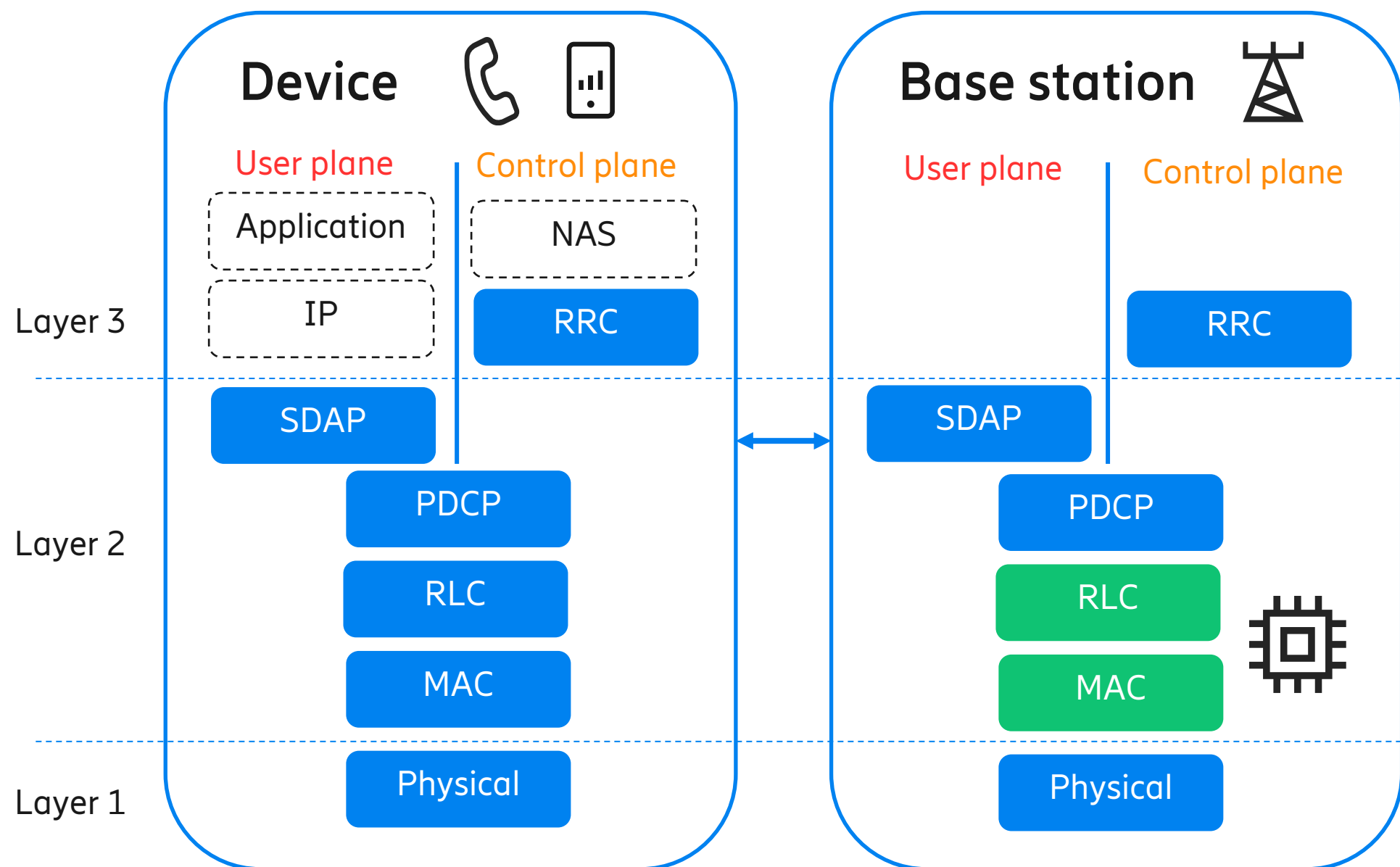
Ericsson Research has assessed the suitability of CHERI for telecommunication systems that require high performance and fault tolerance.



t.eric.sn/3Q1lrjD

Porting effort and performance impact of Arm Morello on RLC and MAC benchmarks

Fredrik Hessner, Håkan Englund, Merve Gülmez, Peter Svensson



Radio Link Control (RLC) – concatenate, segment and reassemble RLC Packet Data Units (PDUs) to/from MAC/PDCP data units; reorder, duplicate detection, RLC re-establishment
Medium Access Control (MAC) – map logical and transport channels; resource allocation; scheduling and priority; error correction; multiplexing data flows

Porting effort

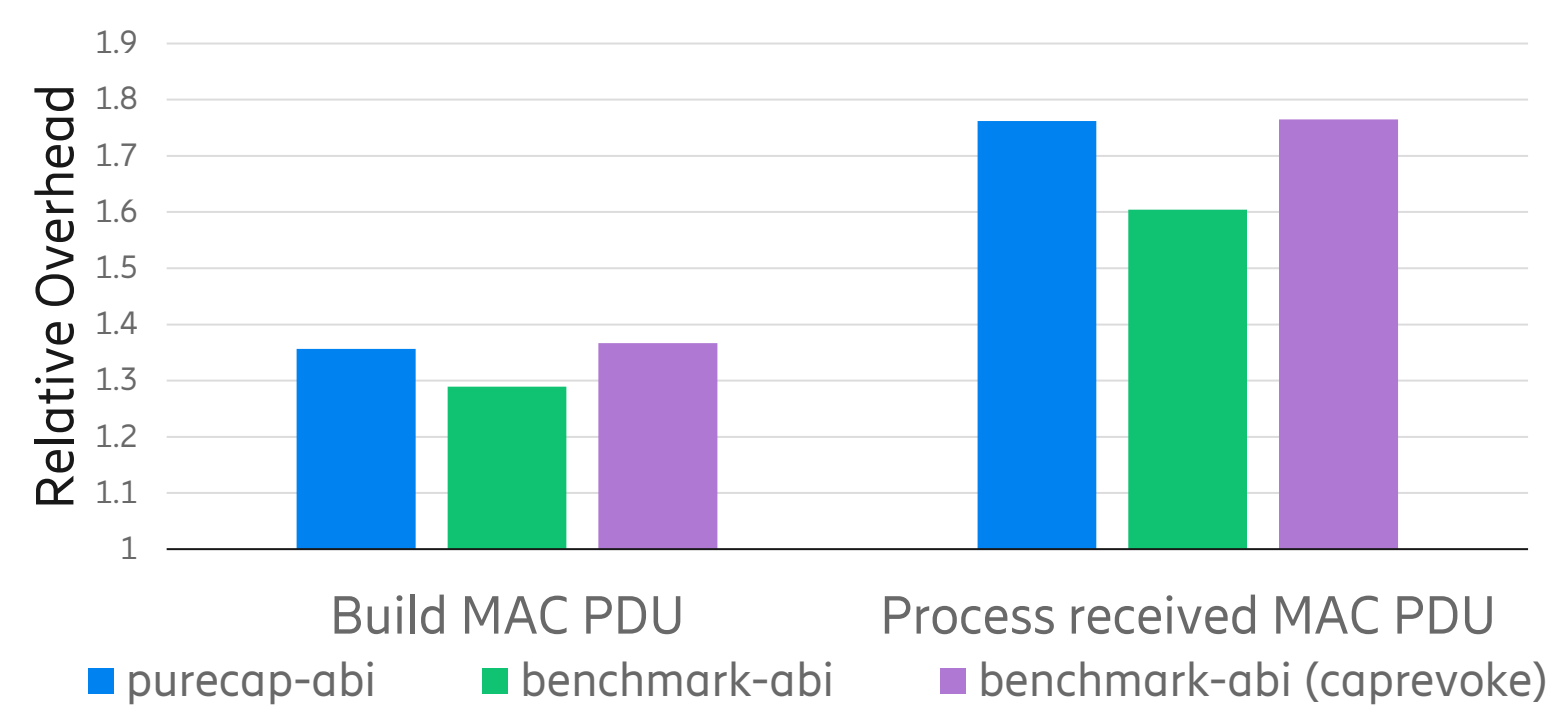
CHERI-related benchmark changes:

- Less than %1 LoC changes to introduce capabilities
- Includes CHERI-related changes to custom heap allocator

BSD-related changes:

- Removal of Linux Tracing Tool Next Generation (LTTNG).
- Naming differences between Linux and BSD

Performance using RLC and MAC benchmarks



Overhead relative to non-capability baseline using hybrid mode application and kernel. All benchmarks run in purecap mode on purecap kernel. Max std = %4.9

CHERI-extension for conditional capabilities preventing uninitialized memory accesses

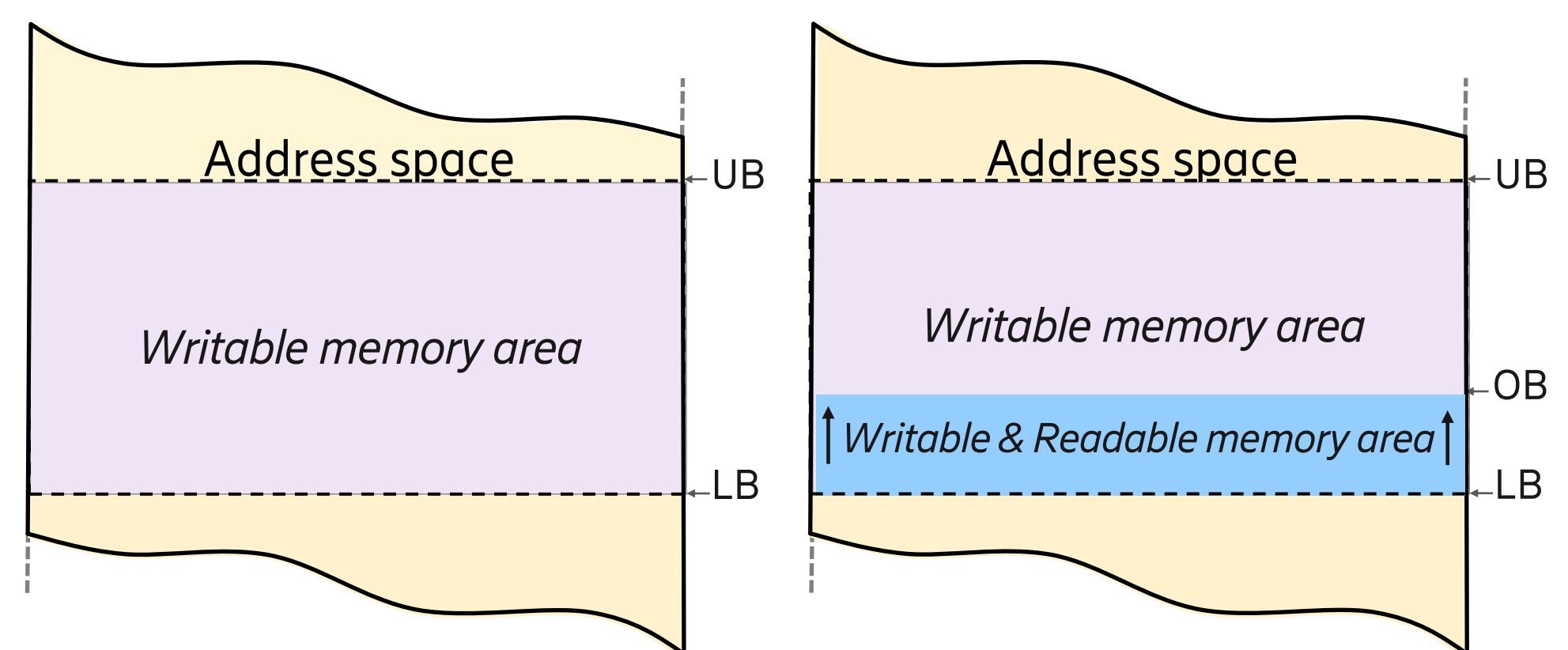
Merve Gülmez, Håkan Englund, Jan Tobias Mühlberg, Thomas Nyman

Enforce memory access policies based on prior operations

- Write-before-Read – write memory at least once before reading
- Operation-specific bound tracks area for which condition is fulfilled
- Operation bound compressed into top 16 bits of address

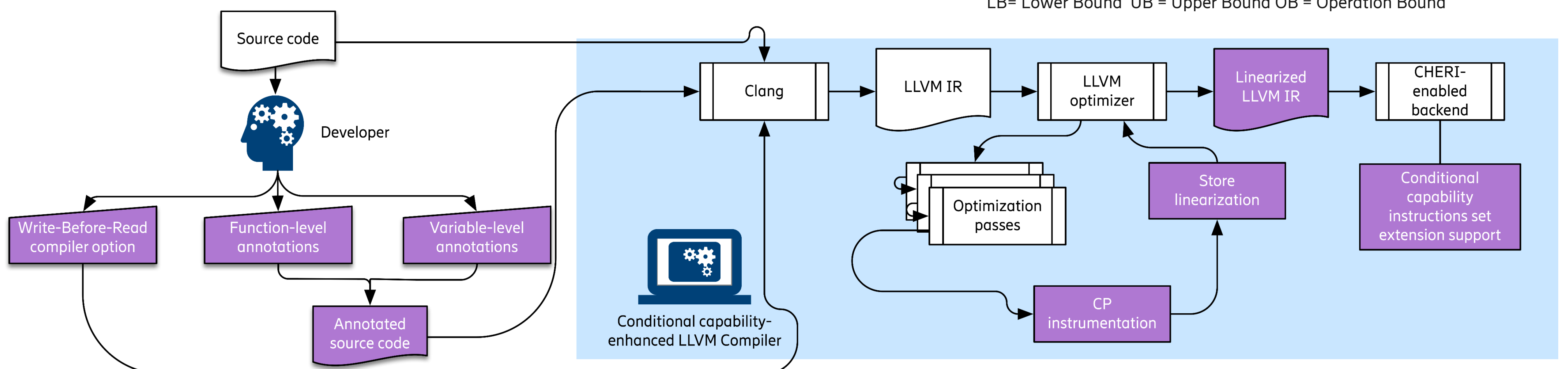
Evaluated using CHERI-Flute softcore and QEMU-based simulation

- Coremark: %3.5 performance overhead in addition to CHERI
- Juliet Test Suite: 100% detection with \approx 1% false positive

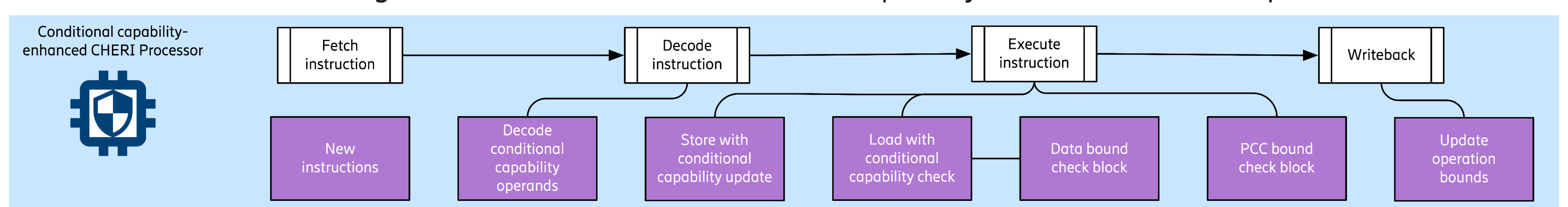


Write-before-Read capability state transitions

LB= Lower Bound UB = Upper Bound OB = Operation Bound



High-level overview of the conditional capability-enhanced LLVM compiler



Conditional capability-enhanced CHERI processor